

## **AMENDMENTS TO THE CLAIMS:**

This listing of claims will replace all prior versions and listings of claims in the application:

1-4. (Cancelled)

5. (Currently Amended) A method for manufacturing a flash EEPROM cell, comprising the steps of:

forming a tunnel oxide layer over a silicon substrate;

forming a floating gate by depositing a polysilicon layer over the tunnel oxide layer;

forming a first dielectric layer over the floating gate;

forming a first control gate by depositing a polysilicon layer partially over the first dielectric layer, thereby exposing at least a portion of the first dielectric layer;

forming a second dielectric layer covering the first control gate and the exposed portion of the first dielectric layer;

forming a second control gate by depositing a polysilicon layer over the second dielectric layer; and

forming a source and a drain in the silicon substrate ~~by ion implantation with a self-aligned etching technique~~, wherein an edge of the first control gate is substantially aligned with an edge of the floating gate and an edge of the source.

6. (Currently Amended) The method as recited in claim 5, wherein ~~[[one]] a~~ sidewall of the first control gate ~~at least partially overlaps~~ is substantially aligned with a respective sidewall of the second control gate.